

In The Claims:

1. (Previously presented) A microprocessor, comprising:

an instruction cache configured to store instructions;

a branch prediction unit;

a trace cache configured to store a plurality of traces of instructions; and

a prefetch unit coupled to the instruction cache, the branch prediction unit, and the trace cache;

wherein the prefetch unit is configured to fetch instructions from the instruction cache until the branch prediction unit outputs a predicted target address;

wherein the prefetch unit is configured to check the trace cache for a match for the predicted target address in response to the branch prediction unit outputting the predicted target address;

wherein the prefetch unit is configured to not check the trace cache for a match until the branch prediction unit outputs the predicted target address; and

wherein in response to the prefetch unit identifying a match for the predicted target address in the trace cache, the prefetch unit is configured to fetch one or more of the plurality of traces from the trace cache.

2. (Original) The microprocessor of claim 1, wherein the branch prediction unit is configured to output the predicted target address in response to a prediction that a branch will be taken.

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